

Wafer Thinning Process and its Critical Manufacturability Requirements

ABSTRACT

Wafer Thinning as a major semiconductor process steps to attain miniaturization of Integrated Circuit or IC. Wafer back grinding up to 70 μm thickness is considered critical due to its fragility. The paper will discuss the definition and establishment of critical equipment check items to lessen the risk of breakage. Equipment covered was an inline wafer back grinding and wafer mounting. The research has used a qualitative approach by applying process mapping to identify critical sub-process steps. Thereafter, the results show the establishment of critical equipment subprocess steps such as grinding, lamination and de taping. Foreign material and alignment control are considered areas for improvement and have incorporated the control at the equipment preventive maintenance. After all the evaluation, wafer thinning process was successfully released and proliferated from development to manufacturing.

Keywords: Wafer, Wafer Thinning; Back grind Tape; Chuck Table condition; Polishing Pad;

1. INTRODUCTION

The development of thinner electronics packages also anticipates the need for thinner architecture inside the Integrated Circuit packages. To attain thinner packages, several enablers such as thinner substrates, mould caps, adhesive bond line and die thickness were introduced. Though, ICs package density should be designed according to its application and its corresponding reliability requirements. The paper will focus on Die thickness as a major enabler for thinner packages and its corresponding manufacturing controls.

The research will then focus on comparing if the current control used for thicker wafers (with greater 100 μm thickness) will still apply to thinner wafers (less than 100 μm). Also, the paper will discuss the results of validating the current equipment set-ups if it can cater 70 μm wafers. The research will help the future IC manufacturing plants to consider the critical areas of the wafer handling system of the wafer back grinding and mounting equipment. Also, the research will help the academe to consider actual manufacturing scenarios to include on their respective semiconductor process syllabus.

2. REVIEW OF RELATED LITERATURE

Die thickness of less than 100 μm and below will be attained by the introduction of specialized wafer thinning process. According to Zhou, et.al, to attain thinning wafer or silicon wafers an ultra-precision grinding machine [1] should carry it out. Nowadays, several issues and requirements are encountered during proliferation from development to the manufacturing phase. The paper will discuss the several key process requirements to attain stress-free wafer thinning to 70 μm and 50 μm die.

Wafer thinning process revolves on the development of grinding wafers up to 70 μm and 50 μm final thickness. Wafer back grinding serves as the critical process of thinning were consists of three major steps: coarse grinding, fine grinding and Chemical Mechanical Polishing or CMP [2]. As described by Sandireddy, S. and Jiang T. (2005), coarse grind removes silicon faster using large diamond particle size while fine grind is a much slower rate and smaller diamond particle size, which ease up the occurrence of wafer damage. Moreover, an additional step was introduced to increase die strength and decrease the risk of die crack [3]. An additional step was called CMP or Chemical Mechanical Polishing, which acts as stress relief, reduces surface roughness and die related defects [4]. However, all processes have their weaknesses. CMP, which introduced very small particles to polish the silicon layer of the wafers. Critical particle control should be implemented to eliminate micro scratching and worse is wafer breakage [5]. Additional studies from Chia et. al. (2018), states that any unevenness of the die after grinding was the main factor of low die strength that make it's susceptible to cracks. [6] Lastly, Marks et. al. (2014), cited additional requirement for thinner dies, which is Total Thickness Variation or TTV, which states the difference between the maximum and minimum die thickness. TTV is an important indication of the grinding machine accuracy [7]. The paper will discuss the requirements of manufacturing before and during wafer back grinding of the wafer thinning process.

The auxiliary process such as back grind taping is needed for wafer thinning. BG tape was laminated on top of the wafer to support cushioning during the grinding process. Excessive friction can induce cracks on the active layer and will affect its electrical performance. As discussed by Abdelnaby, et. al. (2011), the friction or the amount of heat affects the reliability of the wafer [8]. Nowadays, wafer back grinding machines are already in line with wafer mounters wherein dicing tapes or die to attach films were laminated before wafer sawing. The last process on inline grinders and mounters was the BG tape peeling, wherein BG tape was removed from the wafer front side.

3. ACTUAL EVALUATION

3.1 Materials

Wafer Thinning will focus on 200 mm wafer size using an ultrafine back grind machine. The equipment will have a full wafer back grind process: coarse, fine and CMP; and connected to a full wafer mouter process. DAF lamination will be done on the wafer mouter then BG tape will be de-tape from its front side. Final wafer thickness will be 70 μm . Process Flow is shown in Fig. 1:



Fig. 1. Wafer preparation processes

Two different back grind tapes or BG tapes with different adhesion strengths were used: Non-UV and UV type tape. BG tapes were evaluated to check if the adhesion would affect the BG tape peeling process that can lead to wafer crack.

3.2 Equipment

The equipment used was a commercially available grinder (Accretech, Model PG200) [9]. Grinding wheels was also from Accretech [10]. The final thickness of the wafer is 50-70 μm .

3.3 Procedure

To established critical manufacturability requirements for wafer thinning, several process and equipment critical points were studied.

- ✓ Wafer BG Tape Lamination
- ✓ Chuck Shape
- ✓ Grinding Spindle 1 & 2 Angle
- ✓ Chuck Vacuum Condition
- ✓ Wafer Handling parts condition
- ✓ UV function
- ✓ CMP Polishing Pad
- ✓ BG tape peeling station

4. RESULTS AND ANALYSIS

4.1 Wafer BG Tape Lamination

Wafer BG Taping is the first process to consider in handling thin wafers. One critical parameter was Applying Roller pressure. Applying Roller Setting (200mm) is decreased by 10% of its original setting to minimize the lamination pressure. Also, Wafer BG tape edge cutting should be monitored which may incur edge chippings during Back grinding of thin wafers. Dull Cutter should be replaced prior worn-out to eliminate rough edge cutting.

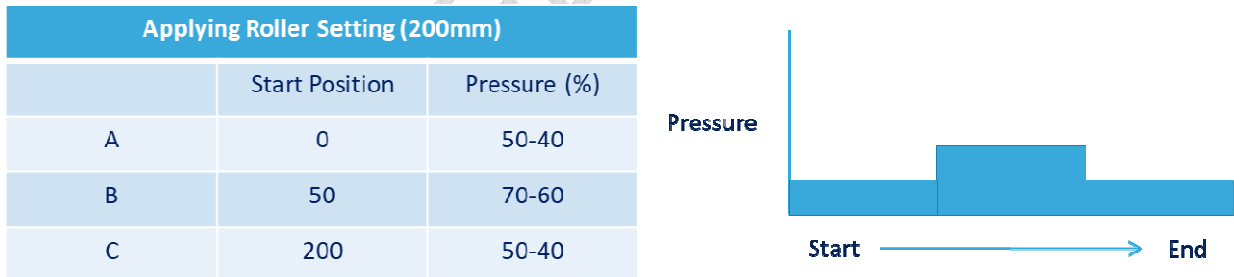


Figure 2. Recommended Lamination Settings

4.2 Chuck Shape

Chuck Shape is a mechanical characteristic to check planarity of chuck table. This is to define chuck centre height difference compared to chuck edge. The individualities will play a major role on the wafer thickness variation and planarity of the silicon wafer that to be ground. The specification of $\pm 5\mu\text{m}$ will define the total thickness variation or TTV requirement of the wafer back grinding of $\pm 10\mu\text{m}$.

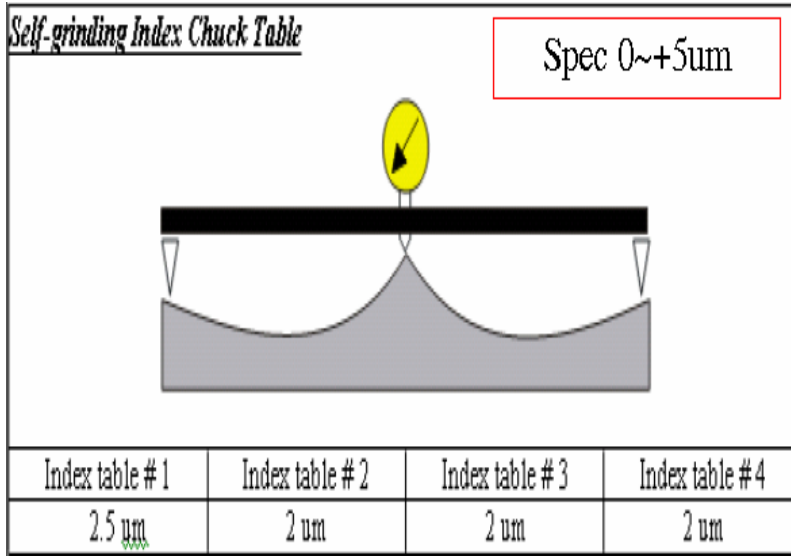


Figure 3. Recommended Lamination Settings

4.3 Grinding Spindle 1 & 2 Angle

Grinding Spindle Angle adjustment is also necessary to ensure good TTV was achieved after wafer back grinding. Compared to chuck shape, spindle angle is also critical since it will drive the cutting angle of the wafer thus planarity is critical to meet the TTV requirements. Table 1 shows the before and after adjustments.

Table 1. Before and After Grinding Spindle Angle Adjustment

Adjustment	Grinding Spindle 1			Grinding Spindle 2		
Before	0	-10	-25	0	-4	-19
After	0	-3	-25	0	-3	-25

Before the spindle angle adjustment, -4 and -25 angles have 6um difference on both Spindle 1 and 2 grinding wheels. After adjustments, shown in Figure 4, indicates that no differences on both spindle in which the grinding angles for both spindles will have the same removal rate for coarse and fine grinding. Lastly, no differences between spindle angles will eliminate potential TTV impact on final wafer thickness.

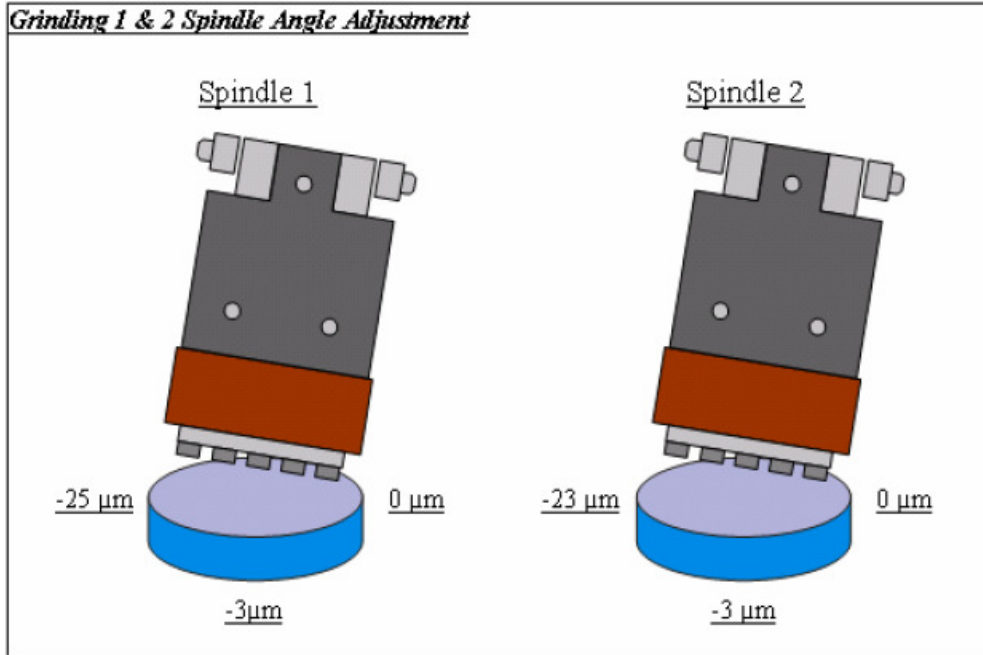


Figure 4. Grinding Spindle Angle Adjustment

4.4 Chuck Vacuum Condition

After ensuring the top and bottom surface alignment, next will be the wafer handling areas. The most critical wafer handling part will be the chuck table, where the wafer seats during wafer back grinding. Chuck table is normally on porous form wherein vacuum will ensure covers the complete backside. One critical characteristic of the chuck table is its vacuum condition. It defines the wafer suction power of the chuck table. Figure 5 shows that the porous area should not have to clog to maximize the vacuum efficiency of the chuck area.

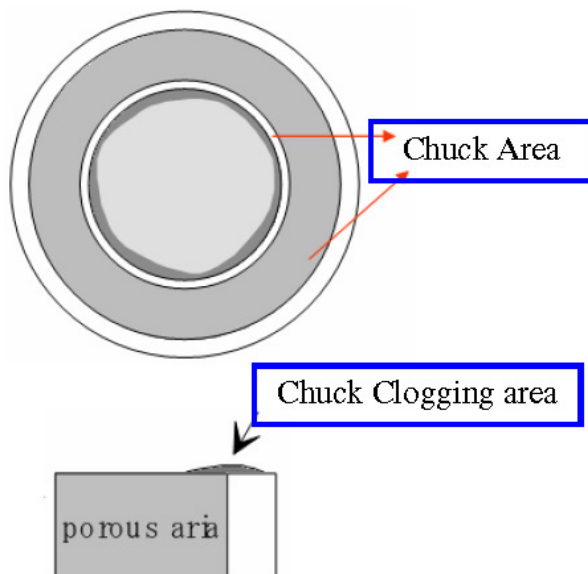


Figure 5. Chuck Table Condition

The in-line equipment typically has 4 chuck tables to have at least one wafer on each part of the wafer back grind process. Based on the assessment, indicated in Table 2, the chuck table has a clogged area wherein cleaning is necessary to ensure vacuum coverage and will eliminate detached wafer during the back grinding process.

Table 2. Before and After Grinding Spindle Angle Adjustment

Chuck Table	Vacuum	Release
1	90% good	Good
2	Good	Good
3	Good	Good
4	Good	Good

3.5 Wafer Handling Parts Condition

Another critical handling part was the spinner chuck table, in which wafer seats during wafer cleaning. After the assessment, the spinner table has damage on the wafer edge surface that may incur wafer breakage during the spinning process or H2 place to spinner station, specifically for thinner wafers after polishing. Figure 6, shows that the spinner table should not have any cracked area that can initiate an uneven table and later results to wafer breakage.

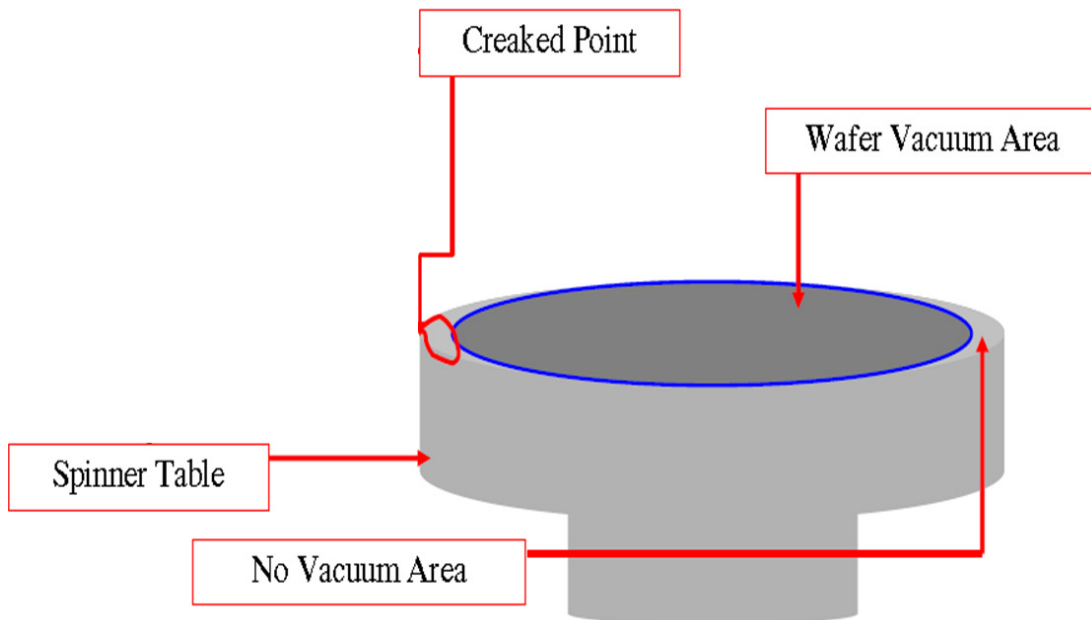


Figure 6. Spinner Chuck Table Condition

4.6 UV Function Condition

UV Condition is important to ensure the detaining process is effectively performed, given that ASIC die is using a UV type BG tape. After the assessment, UV type BG tape is needed for

wafer thinning process due to higher adhesion strength during wafer back grind. The adhesion strength will ensure the cushioning of wafer thus will eliminate the wafer detachment during grinding

4.7 CMP Polishing Pad

The third back grinding process is highly critical since the thickness is already below 75um, thus a need for good process handling is necessary. CMP uses polishing pads and slurry to attain mirror-finished back grind. After the assessment, polishing pad to be used should not have a slurry slot that could lead to the stocking of hardened slurry and will incur foreign material or worst wafer breakage, as shown in Figure 7.

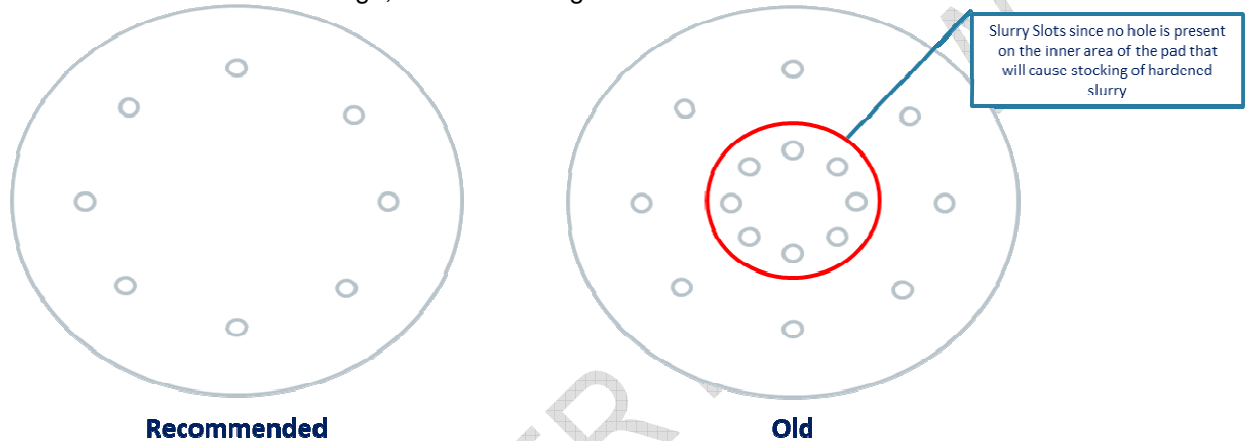


Figure 7. Polishing Pads Condition

4.8 BG tape peeling station

The last step for in-line back grind and mount equipment is the BG tape peeling station. Since we are dealing on removing BG tape on top of a very thin wafer. Even though the UV BG tape has very light adhesion after radiation, handling will still be carefully established. After the validation, the peeling roller defines the evaluation shows that the success of the peeling and elimination of dislodging of the wafer. The phenomena are that the BG peel tape should exactly touch the edge of the thin wafer and not to touch the dicing tape or die to attach film that can dislodge the wafer during peeling.

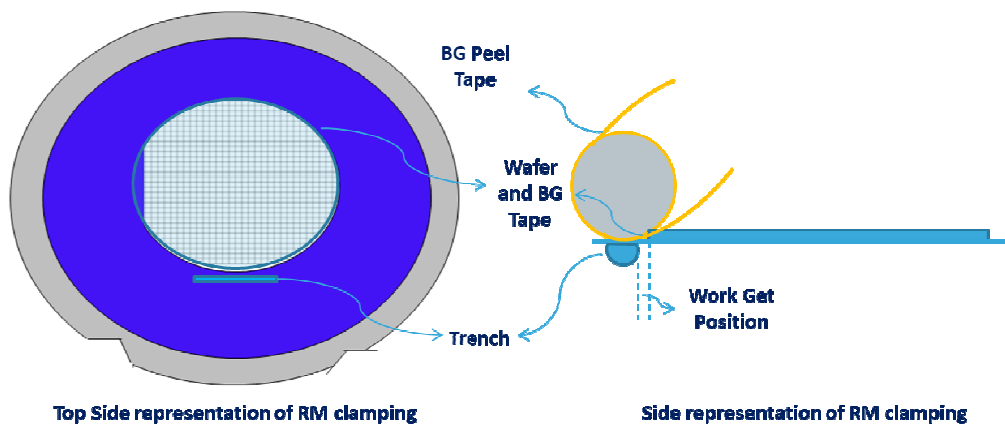


Figure 8. BG Tape peeling station condition

5. CONCLUSION

Wafer thinning process should be carefully defined by establishing process and equipment requirements. Critical items will start from wafer back grind tape lamination, wafer back grind process and its handling system and up to wafer back-grind tape peeling. Foreign Materials, process alignments and clogging are critical items for its handling steps. BG tape lamination and peeling should be defined to eliminate wafer breakage due to potential wafer dislodge at process step. Lastly, UV back-grind tape should be used to ensure high adhesion during wafer back-grinding for cushioning while lower adhesion during the peeling process.

To summarize, equipment should be on good process alignment and will be free of foreign materials and clogging in order not to reduce the risk of wafer breakage of 70 μm thickness.

COMPETING INTERESTS DISCLAIMER:

Authors have declared that no competing interests exist. The products used for this research are commonly and predominantly use products in our area of research and country. There is no conflict of interest between the authors and producers of the products because we do not intend to use these products as an avenue for any litigation but the advancement of knowledge. Also, the research was not funded by the producing company rather it was funded by the personal efforts of the authors.

Ethic: NA

Consent: NA

REFERENCES

1. Zhou, L., et. al. A study on the diamond grinding of ultra-thin silicon wafers, Journal of Engineering Manufacture 2011
2. Mizushima Y, et.al.. Impact of back-grinding-induced damage on Si wafer thinning for three-dimensional integration. Japanese Journal of Applied Physics 2014
3. Sandireddy, S., Jiang, T. Advanced Wafer Thinning Technologies to Enable Multichip Packages, 2005 IEEE Workshop on Microelectronics and Electron Devices, 2005
4. Feeney, P. Shumway, L., Process Optimization of Grinding and CMP for Thinning of Si, ICPT 2012 - International Conference on Planarization/CMP Technology
5. Benner, G.et. al., Reduction of CMP-induced wafer defects through in-situ removal of process debris, 2011 IEEE/SEMI Advanced Semiconductor Manufacturing Conference
6. Chia, L.C. et. al, Characterization of Silicon Die Strength with Different Die Backside Unevenness Location, 38th International Electronic Manufacturing Technology Conference, 2018

7. Marks, et. al., Characterization Methods for Ultrathin Wafer and Die Quality: A Review, IEEE Transactions On Components, Packaging and Manufacturing Technology, Vol. 4, No. 12, December 2014
8. Abdelnaby, A.H. et. al., Numerical simulation of heat generation during the back-grinding process of silicon wafers, 2012 IEEE Workshop on Microelectronics and Electron Devices
9. Accretech, Polish Grinders, <https://www.accretech.jp/english/product/semicon/polish/index.html>
10. Accretech, Polish Grinders and Consumables, https://www.accretech.jp/english/product/semicon/polish/files/pg3000rmx_e.pdf

UNDER PEER REVIEW