Original Research Article

Die Crack Resolution Through Pick-up Process Optimization for BGA Package

ABSTRACT

With the new devices and new technologies in semiconductor industry are getting more challenging to process because issues are unavoidable especially on thin dies. The paper is focused on the improvement done in ball grid array (BGA) substrate package assembly to address the quantity of rejection of die crack during die picking at die attach process station. High pick force and high needle top height found out during pick-up process is the main root cause of die crack. Parameter optimization particularly for die picking with the combination of pick force and needle top height parameter was done to eliminate this type of issue after die attach process. With this die attach process improvement, a reduction of 100 percent of die crack was achieved. For future works, the improvement and learnings could be used for devices with similar requirement.

Keywords: BGA; die crack; pick force; pick-up process; silicon die.

1. INTRODUCTION

To keep-up with the fast-changing technology and development in semiconductor industry, one should be flexible and resourceful in adapting to change in order to have a very good impression from the eventual customer. This is one of the biggest challenges for any semiconductor company in order to maintain its competitive market position and value. Contrariwise, failure to provide customer expectation will result to possible business failure.

BGA packaging technology are continously developed and improved to deliver high quality and robust products for various applications. A common direction of semiconductor manufacturing companies is to increase the production yields and maintain high quality products while minimizing the wastage and assembly rejections. With the new and continous technology trends and breakthroughts, challenges in assembly manufacturing are unavoidable [1-4]. Die attach process is responsible in picking a silicon die on a wafer tape to a substrate or carrier. This paper presents a solution and improvement done to process this type of assembly manufacturing reject which is die crack by optimizing the pick parameter of pick force and needle top height. Pick force is the amount of additional pressure applied during picking the silicon die with the help of vacuum to picked while needle top height is a parameter wherein the needle push upward or to eject the silicon die. Fig. 1 shows the actual unit of die crack.

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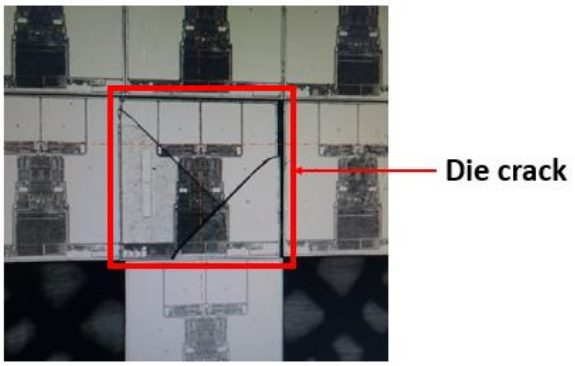

Fig. 1. Actual reject manifestation of die crack

2. METHOD AND RESULTS

A typical assembly process flow for the BGA package device in focus, starting with the pre-assembly to singulation process is shown in Fig. 2. Highlighted is the process where the issue was encountered. important to note that assembly process flow varies with the product and the technology [5-7].

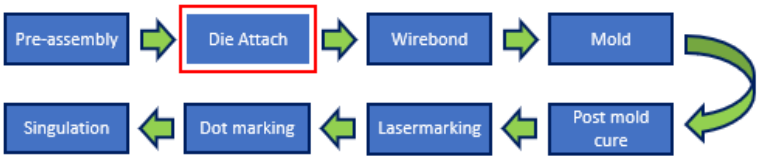

Fig. 2. Device process flow

Die crack was the top major assembly reject in die attach process for the device in focus, and this was seen during the lot processing on the development stage of the device. One of the challenge is to process this type of technology with a thin die thickness of 70 microns (µm). This die crack reject is caused by a high needle top height and high pick force during the die picking process. Fig. 3 illustrates the pick-up process.

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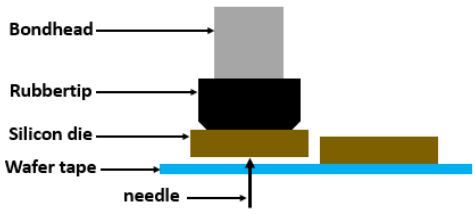


Fig. 3. Pick-up process representation

The process starts with picking the semiconductor die from a wafer silicon tape. The most common method used in die bonding: First, is when the ejector needle push up the target semiconductor die from the wafer silicon tape; then is picked by a rubber tip or pick-up tool as shown in fig. 3. With this pick process, Fig. 4A shows the die crack pick process while Fig. 4B is the actual die crack during picking the silicon die. High pick force and needle top height found out that this parameter fully induced on the defect manifestation of die crack.

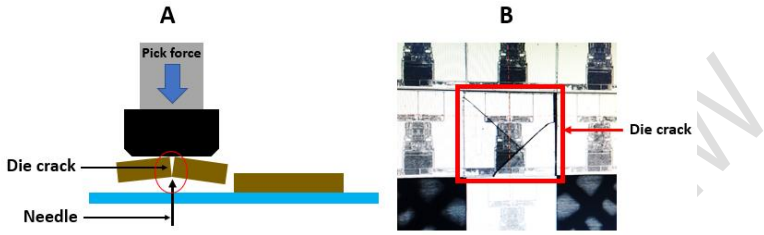


Fig. 4A. Die crack pick-up process; 4B. Actual die crack during picking of silicon die

An improved and enhanced process solution in die attach process is widely done with the combination of pick force and needle top height parameter optimization. The needle used is usually a plastic type and this was normally used in all semiconductor industries. With the combination of pick force and needle top height parameter optimization, no die crack occurrence is seen after implementing the improvement in die attach process. Fig. 5. shares the evaluation table of pick force and needle top height. The result of needle top height parameter from 0.4mm to 0.7mm has an evidence of die crack while 0.2mm to 0.3mm is the best parameter to used without die crack and the die is properpy picked and placed on the leadframe or substrate carrier. The result of pick force parameter from 1.1N (newton) to 2N (newton) has an evidence of die crack while 0.5N to 1N is the best parameter to used without die crack.

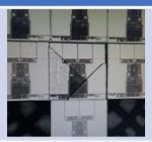
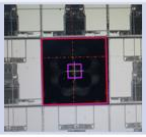
Parameter (needle top height and pick force)	Response	Remarks
Needle top height 0.6mm - 0.7mm Pick force 1.6N – 2N		With evidence of die crack
Needle top height 0.4mm – 0.5mm Pick force 1.1N – 1.5N		With evidence of die crack
Needle top height 0.2mm – 0.3mm Pick force 0.5N – 1N		No die crack

Fig. 5. Shows the evaluation table of pick force and needle top height

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Comment [JMR26]: the pick

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The optimized parameter would eventually have a good reliability test and a good die shear strenght. With this optimized pick for and needle top height would properly placed on the leadframe or substrate carrier without die crack occurrence. A 100 percent improvement shared in Fig. 6 was achieved for die crack occurrence. ote that actual parts per million (PPM) level are intentionally not shown due to confidentiality.

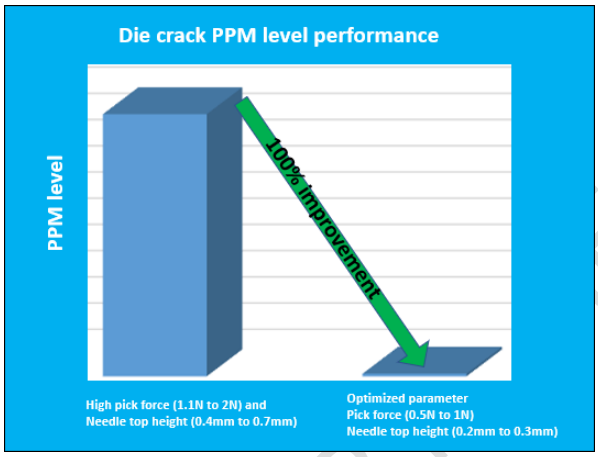

Fig. 6. Improvement in the die crack reduction performance

3. CONCLUSION AND RECOMMENDATION

Die crack mitigation was successfully realized through comprehensive die attach process characterization and optimization for BGA device. Parameter optimization particularly for pick-up process with the combination of pick force and needle top height parameter were employed, resulting to 100 percent improvement on die crack occurrence reduction. The pick parameter optimization in this study could be used for future works on other BGA products with similar configuration. Comparison of existing works and other studies should also be included for added analysis. Worth noting is that continuous process improvement is important to sustain the high-quality performance of semiconductor products and their assembly manufacturing. Studies and learnings shared in [8-10] are helpful in reinforcing robustness and optimization of assembly processes particular at die attach process.

REFERENCES

1. Liu Y, et al. Trends of power electronic packaging and modeling. 10th Electronics Packaging Technology Conference, Singapore; December 2008.
2. Saha S. Emerging business trends in the semiconductor industry. Proceedings of PICMET '13: Technology Management in the IT-Driven Services (PICMET). USA. 2013;2744-2748.
3. Hwang J. Solder paste in electronics packaging: technology and applications in surface mount, hybrid circuits, and components assembly. Ven Nostrand Reinhold, New York, USA; 1989.
4. Yeap LL. Meeting the assembly challenges in new semiconductor packaging trend. 34th IEEE/CPMT International Electronic Manufacturing Technology Symposium (IEMT). Malaysia. 2010;1-5.

Comment [JMR28]: strength

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5. Coombs C, Holden H. Printed circuits handbook. 7th ed., McGraw-Hill Education, USA; March 2016.
6. Harper C. Electronic packaging and interconnection handbook. 4th ed. McGraw-Hill Education, USA; 2004.
7. May GS, Spanos CJ. Fundamentals of semiconductor manufacturing and process control. 1st ed., Wiley-IEEE Press, USA; May 2006.
8. Kahler J, et al. Pick-and-place silver sintering die attach of small-area chips. IEEE Transactions on Components, Packaging and Manufacturing Technology. 2012;2(2).
9. Rodriguez R and Gomez FR. Rubber-tip design improvement for die crack elimination at diebond process. Journal of Engineering Research and Reports. 2020;12(2);1-5.
10. Xian TS, Nanthakumar P. Dicing die attach challenges at multi die stack packages. 35th IEEE/CPMT International Electronics Manufacturing Technology Conference (IEMT). Malaysia. 2012;1-5.