Original Research Article

Addressing Delamination through Advanced Semiconductor Die Design

ABSTRACT

Innovations and breakthroughs are continuously driven in semiconductor manufacturing to overcome existing assembly limitations and recurring difficulties. This paper is focused on the resolution of the delamination issue during die attach assembly process. A new design of semiconductor die is presented to establish a robust adhesion or interface between the silicon die and the epoxy material for die attach. The paper provides a specialized design of manufacturing flow for the improved die design through advanced wafer fabrication method and wafer cutting technique. The realization of the advanced silicon die design would ultimately mitigate the delamination issue during die attach process.

Keywords: Delamination; die attach process; silicon die; wafer.

1. INTRODUCTION

The application of sintering glue or epoxy in silicon die attach process of quad-flat no-leads (QFN) packages requires metallic layer in the backside of the die to enable intermetallic connection between silicon die and sintering glue. Gold (Au) plated on the silicon backside is the common practice in terms of backside coating. Organic or non-metal does not create sintering with the glue, thus it will only cause delamination between interfaces. In addition, the presence of organic compound in leadframe such as anti-epoxy bleed-out or silicon material produces "hydrophobic effect" to the glue which restricts the even wetting of the glue to the surfaces. Studies on delamination and anti-epoxy bleed-out are shared in [1-5]. Die attach delamination in QFN packages is the separation of die attach material to silicon die and leadframe pad.

A scanning electron microscope (SEM) image photo in Fig. 1 shows the cross-sectional view of a die that is attached to a sintering glue. The backside which is Au-plated holds good intermetallic connection with the glue while delamination is observed on the junction (bare silicon/non-metal) part of the die. When aggravated, small delamination may propagate and worsen which can cause a complete delamination of the silicon die to the glue or the delamination may also propagate to the other interfaces inside the QFN packages such as mold-silicon die or mold-leadframe interfaces.

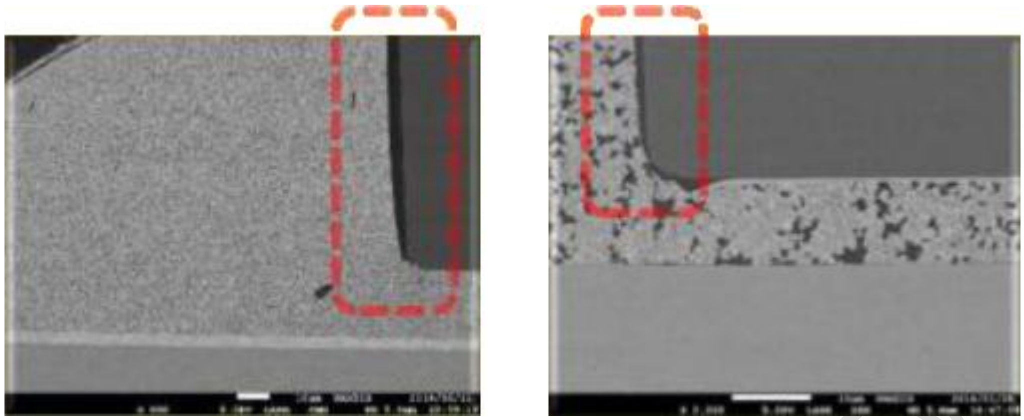

Fig. 1. Cross-sectional view of silicon die interface with glue

The paper is focused on the improvement of the silicon die design that would eliminate the occurrence of delamination on non-metal area such as side junction or sidewall of the die. To fabricate the proposed design, a half-cut is performed on the backside of the silicon wafer then metal such as Au or Silver (Ag) is deposited on the bottom surface. A full cutting will be performed afterwards to separate each individual die. In this design, the sidewall will be incorporated with Au or Ag metal that will enable intermetallic connection of the glue.

2. DESIGN SOLUTION AND METHOD

The formation of epoxy fillet height on the sidewall of the die is a normal behavior of the glue when a die is attached. the surface resistivity of the leadframe, during wetting of the glue, restrict the continuous flow of the glue along the pad thus excess glue will be redistributed to the sidewall of the die wherein there is less surface resistivity. On the other hand, an interface of sintering glue and silicon die, during sintering glue process, will occur on the package.

A silicon die with metallized sidewall design introduced in Fig. 2 is a potential solution to eliminate the delamination formed between the interface of sintering glue and silicon, which occurs on the sidewall. The excess glue building on the sidewall will form intermetallic bond on the metallized sidewall.

Results and discussion

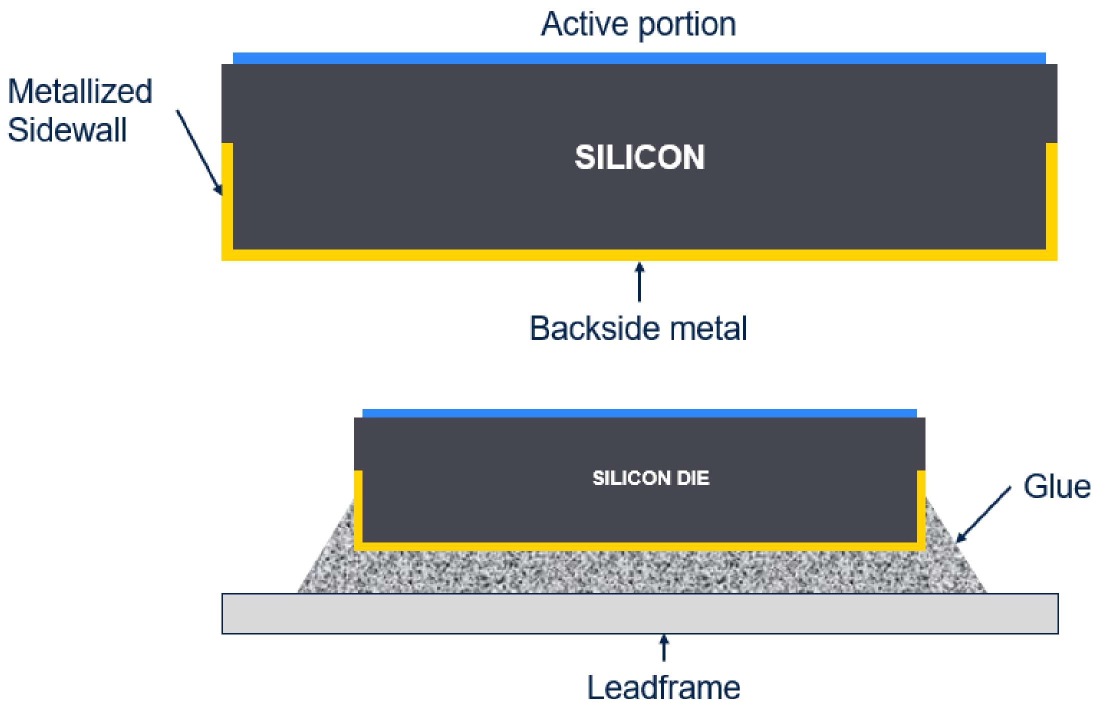

Fig. 2. Advanced semiconductor die construction

The height of the metallized sidewall is recommended to be 75% of the total thickness of the silicon die. Epoxy fillet height can creep/build until 75% on the die, the remaining 25% of the total thickness is for “overflowing guard” between epoxy and active portion of the die.

Fig. 3 illustrates the method of fabricating the metallized die and wafer. A wafer is commonly made-up of silicon material that will be formed into individual slice through series of crystal growth, grinding, sawing and profiling. The active element or microchip on the wafer is formed through different etching and masking technique.

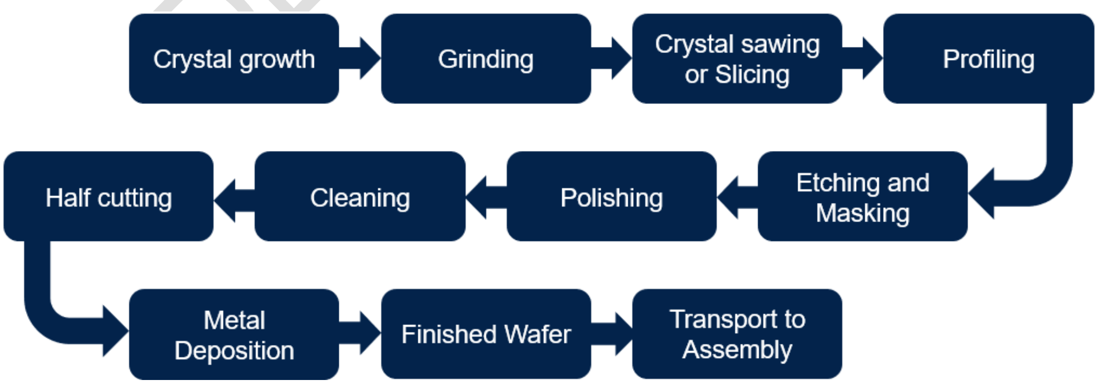

Fig. 3. Wafer fabrication flow

Half-cut or initial cutting is performed in wafer fabrication as shown in Fig. 4. The cutting will be performed at the backside of the wafer which can be done through infrared technology. The size of the blade used to perform the first cut is dependent on the sawing street width. The blade width can have 60-70% of the total saw street. In example: a 70 um blade width can be used for 100 ums saw street. Afterwards, the metal will be deposited on the backside and half-etch area. Technique can be through plating or immersion process.

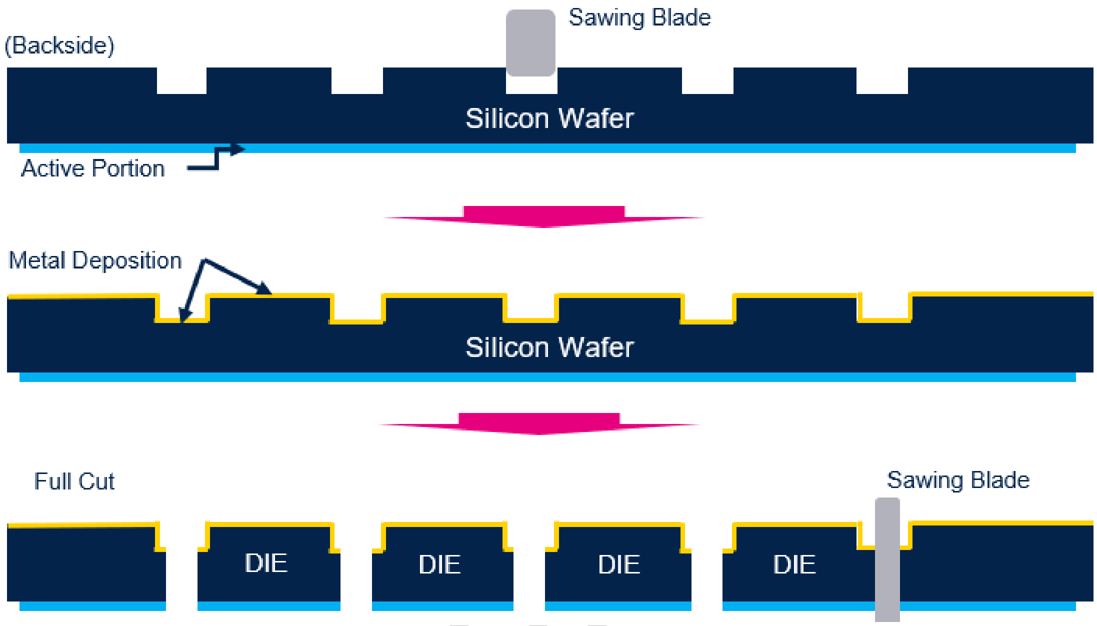

Fig. 4. Wafer cutting technique

To completely isolate each individual die, a full cut is required. This process is performed from the start of the manufacturing process. A blade is required to have a width of 40-50% of the sawing street. A smaller blade is necessary to avoid damaging the metal sidewall of the die during the final cutting or full cutting.

3. CONCLUSION

The paper presented a new semiconductor die design with metallized sidewall for establishing a robust interface with the epoxy die attach material. With the improved design, die attach delamination issues could eventually be mitigated. Future works could adapt the new semiconductor die design to realize a robust die attach process and prevent any die attach related assembly issues. Finally, studies and learnings shared in [6-8] would help reinforce the robustness and optimization of die attach assembly process.

COMPETING INTERESTS DISCLAIMER:

Authors have declared that no competing interests exist. The products used for this research are commonly and predominantly use products in our area of research and country. There is absolutely no conflict of interest between the authors and producers of the products because we do not intend to use these products as an avenue for any litigation but for the

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