Original Research Article

Implementing Single-row Process Plate Design for Pre-encapsulated Leadframe

ABSTRACT

This paper presents the application of an innovative design of wirebond process plate during wirebonding process of thin semiconductor carrier such as the pre-encapsulated leadframe. The implementation of the specialized process plate aims to improve the conventional method of wirebonding from “panel type” to “single-row” design to reduce the occurrence of warpage on thin leadframes. In this study, an 85% reduction for warpage level is achieved after the introduction of the new design of process plate. Furthermore, a significant improvement was observed in production efficiency by eliminating frequent machine alarms and mitigating the time-zero (T0) mold-leadframe delamination during assembly.

Keywords: Wirebond process plate; leadframe; wirebonding process; assembly.

1. INTRODUCTION

Wirebond is one of the process in semiconductor industry for integrated circuit (IC) assembly responsible in attaching the wires to provide electrical connections using thermocompression process although majority of high-end bonding equipment prefer thermosonic bonding due to the delicate structure of some silicon die design. A thermocompression bonding is the combination of force and heat to connect the wire to the silicon bond pads and frames while thermosonic bonding uses ultrasonic, thermal and mechanical energies to form the intermetallic between two metals (semiconductor wire – silicon bond pad, semiconductor wire - leadframe). from both bonding technique, A certain level of temperature is needed to soften the semiconductor wire or “thermal softening” prior a pressure or an ultrasonic energy is applied to the tip of the bonding capillaries. Usually, the temperature is applied to the plate located below the leadframe and silicon die during bonding with a working temperature that ranges from 180 – 200 °C depending on the semiconductor wire to be used (Ag, Au, Cu).

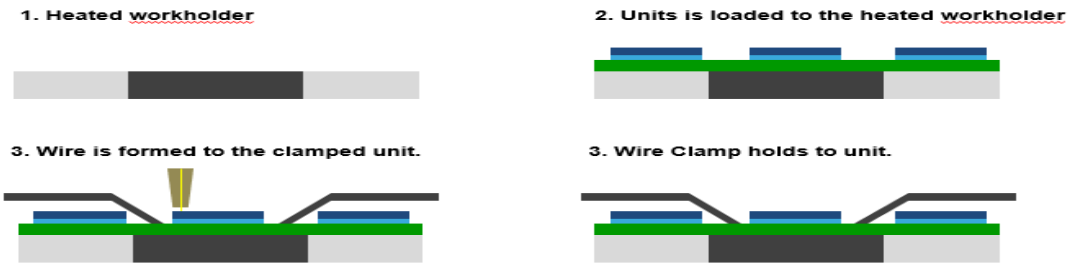

Fig. 1. Mechanical sequence of wirebond equipment machine in forming a wiring connection to the silicon die and frames

Warpage is inevitable to the units that became subjected to heat due to the different coefficient of thermal expansion (CTE) property wherein the material does not follow its

designed shape. Normally, warpage is significant on semiconductor carriers (substrate, pre-encapsulated leadframe, taped leadframes) since this is made-up of multiple material that is mechanically combined. This paper presents the implementation of an improvement in wirebond process plate to mitigate the occurrence of warpage issue on thin-leadframe through changing the design from “panel type” to improved single-row process plate.

2. PROBLEM IDENTIFICATION

A pre-encapsulated leadframe is made-up of chemically etched leadframes that is already covered with a molding compound prior attaching a die, wire and 2nd molding process. the leadframe portion in the material is basically made from a copper material plated with silver or Nickel-Palladium-Gold (NiPdAu) coating wherein the mold that covers the leadframe is fabricated using combinations of polymers and Silica Fillers.

The application of heat during wirebonding process is observed to produce warpage greater than 8 mm acceptable criteria as shown in Fig. 2. The warpage in this study has a significant effect in machine alarm/fallen units from the auto-picker and time-zero (T0) delamination in the mold – leadframe interface.

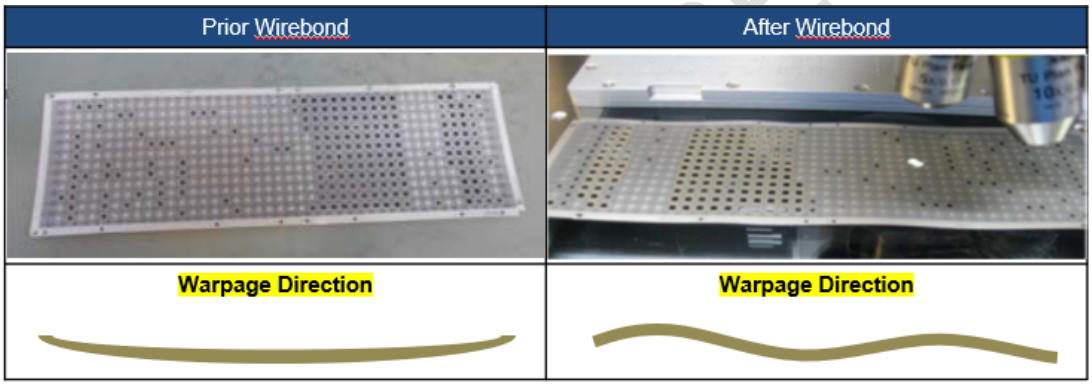

Fig. 2. Warpage comparison before and after wirebonding process

3. PROCESS DEVELOPMENT SOLUTION AND RESULTS DISCUSSION

There are multiple approaches in resolving strip warpage that are known in many assembly sites, however the occurrence of worst warpage in this study is resolved through the improvement and modification in the wirebond process plate material.

The conventional design (panel type) as presented in Fig. 3 covers the whole panel of units during wirebonding. The warpage signature/direction, as observed through process mapping, identified its correlation to the location of process plate footings.

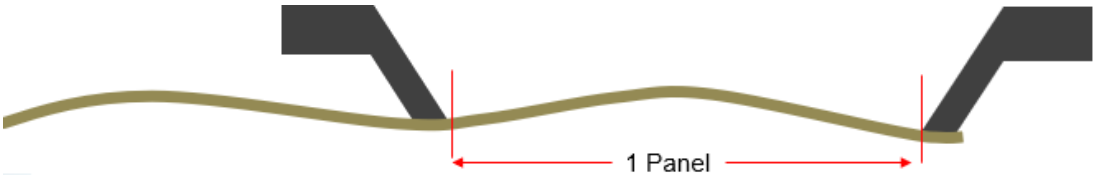

Fig. 3. Warpage Illustration (panel)

The improvement in process plate is done by changing the design to single row process plate. the objective is to minimize the area affected by heat during wirebonding and incorporate a vacuum hole to support the neighbor units as depicted in Fig. 4.

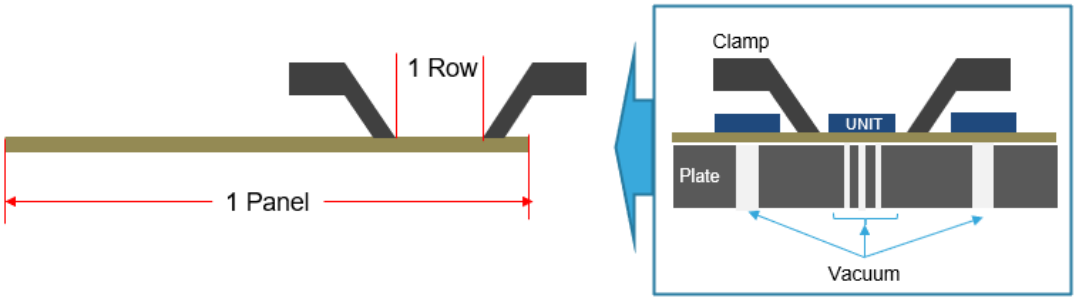

Fig. 4. Wirebond process plate design (single row)

Incorporating the new design of wirebond process plate considers the landing area and size of the footings illustrated in Fig. 5. Landing area is computed from: L= P + (Pt /2), wherein L is the landing area of the clamp, P is recommended package dimension and Pt is the package pitch (tie bar for leadframes). the size or diameter of the footings is recommended to be 60% of the total length of the Pt.

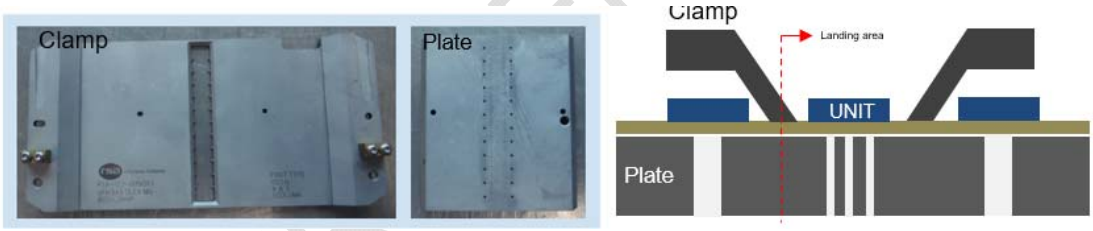

Fig. 5. Wirebond process plate design (landing area)

Upon implementation of the design, an increase in the warpage is observed on the samples although it is below the acceptable limit. There is no delamination observed on the samples after wirebonding samples and no dislodging of strips on the auto picker. There is also no feedback on the succeeding processes for related error and machine stoppage. Figs. 6 to 7 shows the results of the warpage comparison and the actual result after implementation of the new process plate design.

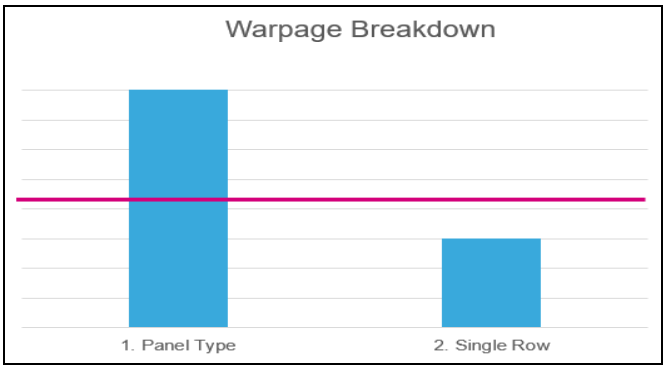

Fig. 6. Warpage Comparison (Panel vs Single)

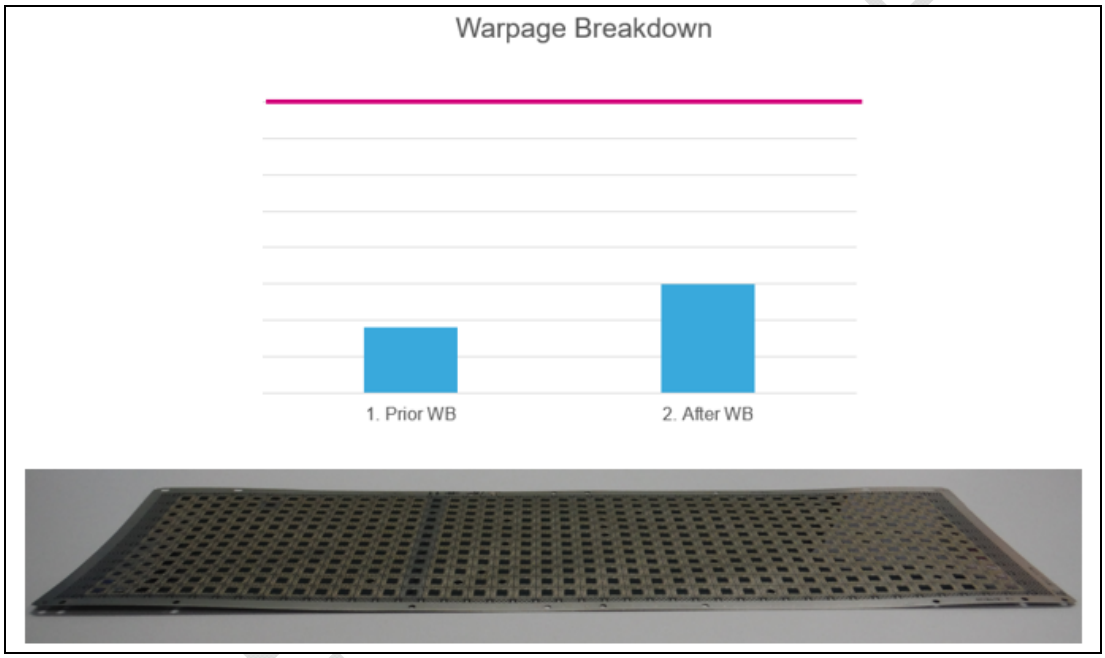

Fig. 7. Actual leadframe strip after implementation

4. CONCLUSION

The paper discussed a process solution and improvement with the innovative wirebond process plate that significantly improved the conventional method of wirebonding from “panel type” to “single-row” design. The new process plate design eventually reduced the occurrence of warpage on thin leadframes particularly the pre-encapsulated leadframe. Ultimately, significant improvement was observed in production efficiency by eliminating frequent machine alarms and mitigating the time-zero (T0) mold to leadframe interface delamination during assembly process. This specialized wirebond process plate is considered a key milestone which could be used for future works on semiconductor packages with similar configuration and requirement.

COMPETING INTERESTS DISCLAIMER:

Authors have declared that no competing interests exist. The products used for this research are commonly and predominantly use products in our area of research and country. There is absolutely no conflict of interest between the authors and producers of the products because we do not intend to use these products as an avenue for any litigation but for the advancement of knowledge. Also, the research was not funded by the producing company rather it was funded by personal efforts of the authors.

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